

FIG. 1

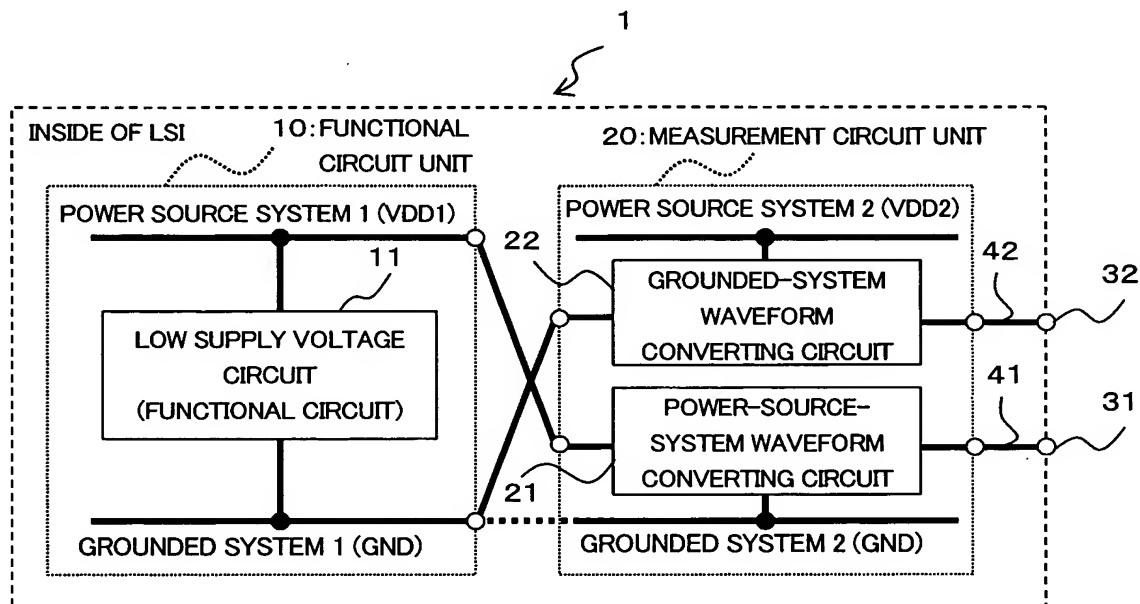


FIG. 2

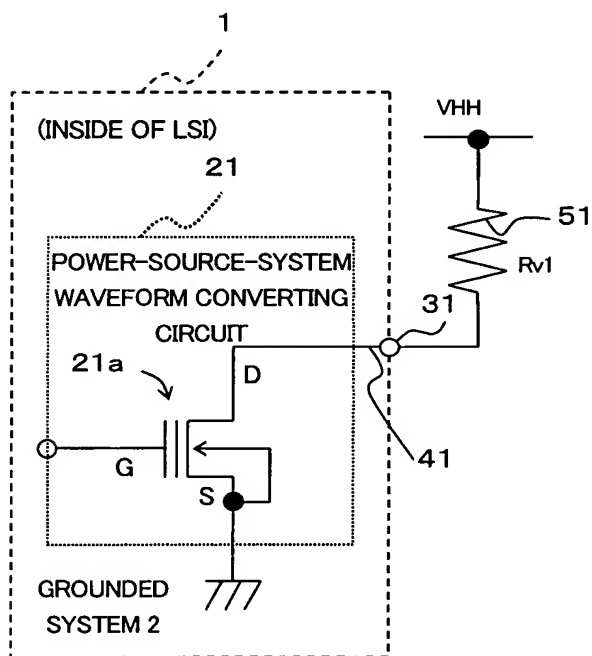


FIG. 3

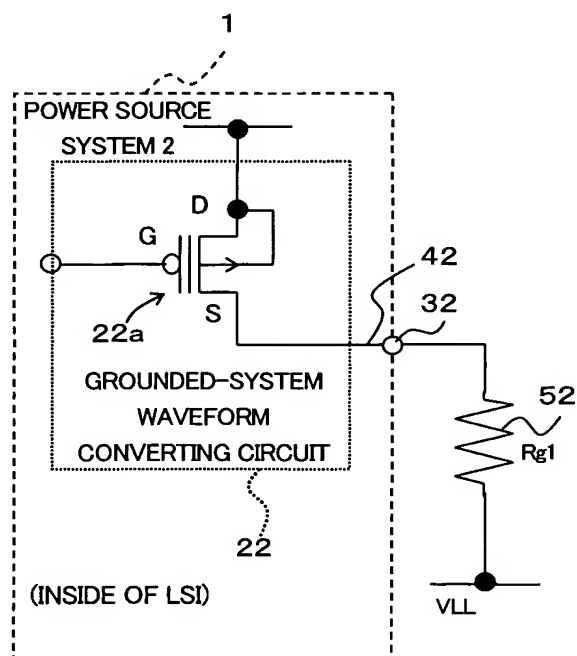


Figure 1 is an equivalent circuit diagram of a semiconductor device. The diagram illustrates the electrical connections between a package and an LSI (Large Scale Integration) chip, focusing on parasitic inductance, resistance, and capacitance (LRC) components.

Package Parasitic LRC: This section, located on the left, represents the parasitic elements of the package. It includes a 1.0V power supply, a 10(11) ohm resistor, and a parasitic LRC component. It is connected to the LSI chip through a "PACKAGE PARASITIC LRC" block.

LSI Chip Internal Structure: The LSI chip is enclosed in a dashed box labeled "LSI 内". It contains several internal components:

- Lower Wiring Parasitic LRC:** A parasitic LRC component located within the LSI chip, connected to the 1.0V supply.
- Upper Wiring Parasitic LRC:** A parasitic LRC component located within the LSI chip, connected to the GND.
- Noise Source:** A noise source is connected to the LSI chip, represented by a circle with a downward arrow.
- VDD2 (1V):** A 1V power supply connected to the LSI chip.
- GND:** Ground connection for the LSI chip.

Output Stage: The output of the LSI chip is connected to a 1.8V power supply and a -0.8V power supply through resistors of 243Ω and 83Ω, respectively. The output voltage is labeled V_{out} . The output stage also includes a "G_out" signal and a "V_out" signal, which are connected to the output resistors.

Other Components: The diagram also shows a "22a" component, which is a diode, and a "21a" component, which is a transistor. These components are connected to the output stage and the 1.8V and -0.8V power supplies.

Figure 10 is a log-log plot showing the impedance of the power plane across a wide frequency range. The y-axis represents Impedance in ohms, ranging from 100n to 10k. The x-axis represents Frequency in Hz, ranging from 1M to 1000G. Three curves are plotted: V-G Impedance (solid line), GND Impedance (dashed line), and VDD Impedance (dotted line). All three curves exhibit a sharp dip around 30MHz and a prominent peak around 400MHz, indicating a resonance or anti-resonance point in the power plane's impedance profile.

FIG. 8

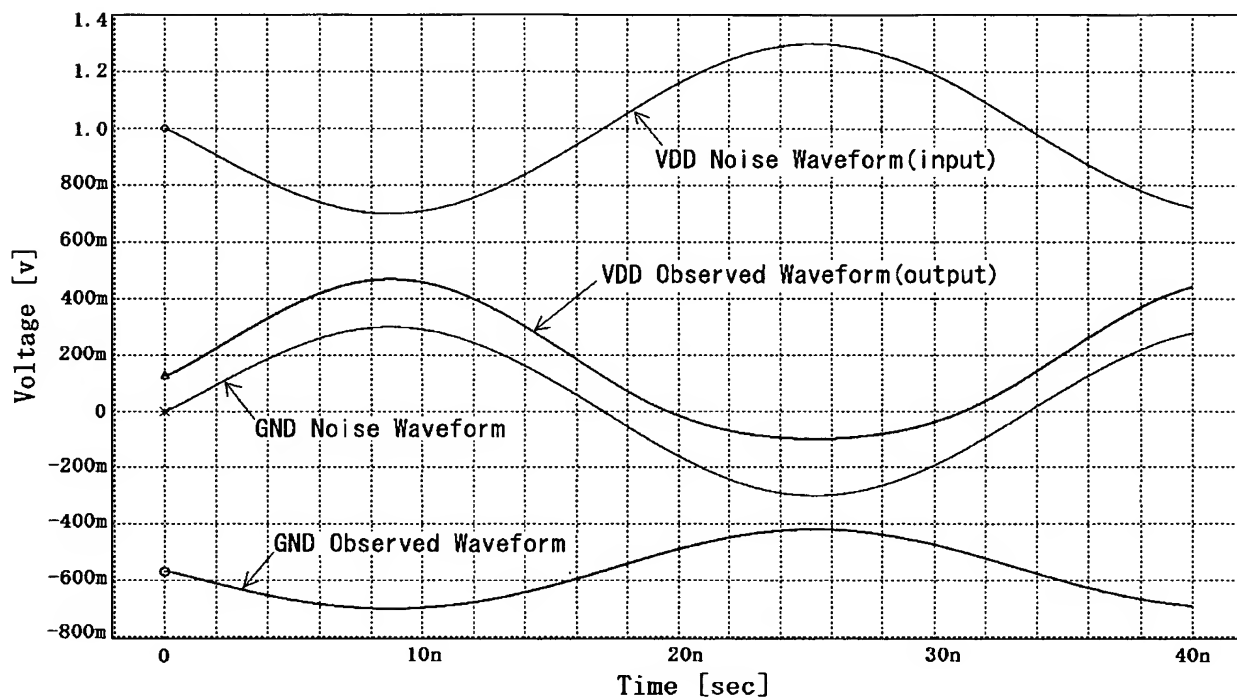


FIG. 9

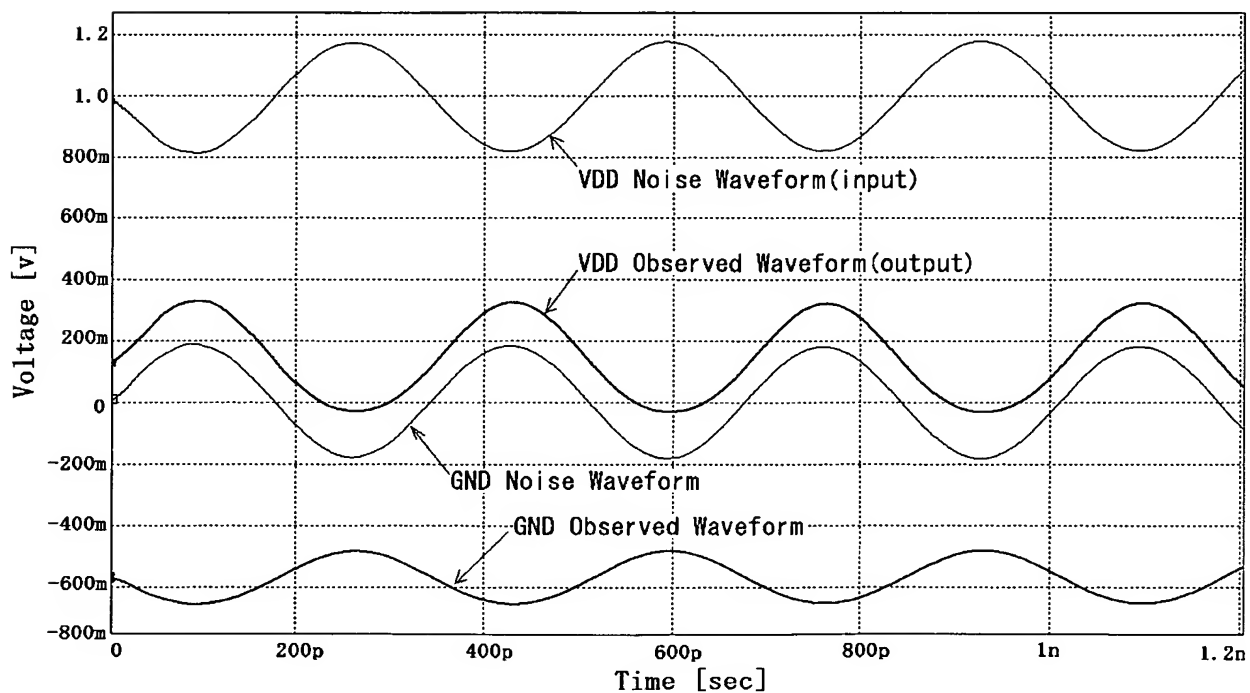


FIG. 10

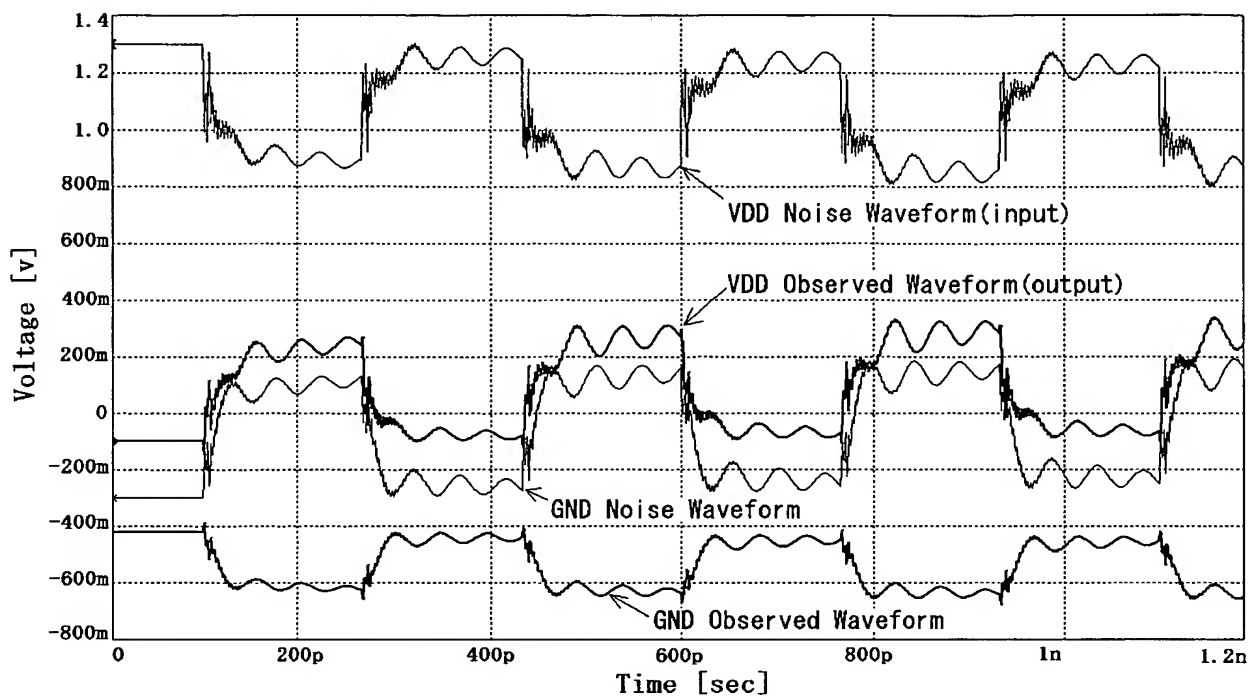


FIG. 11

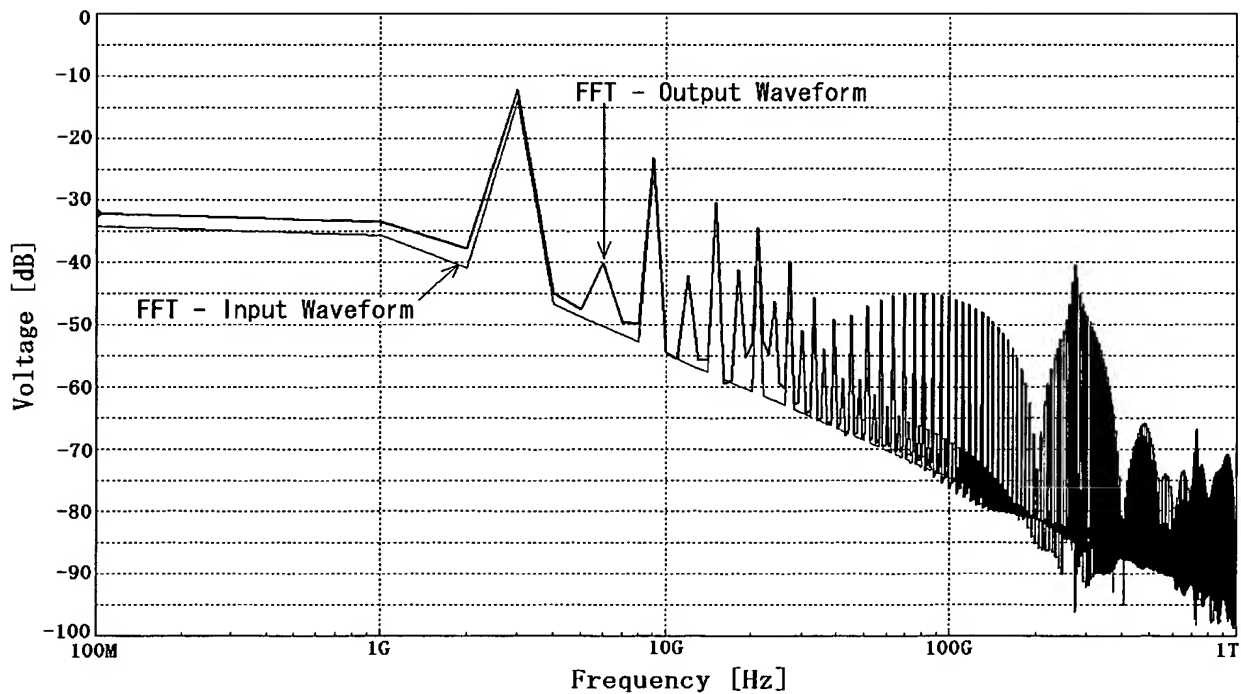


FIG. 12

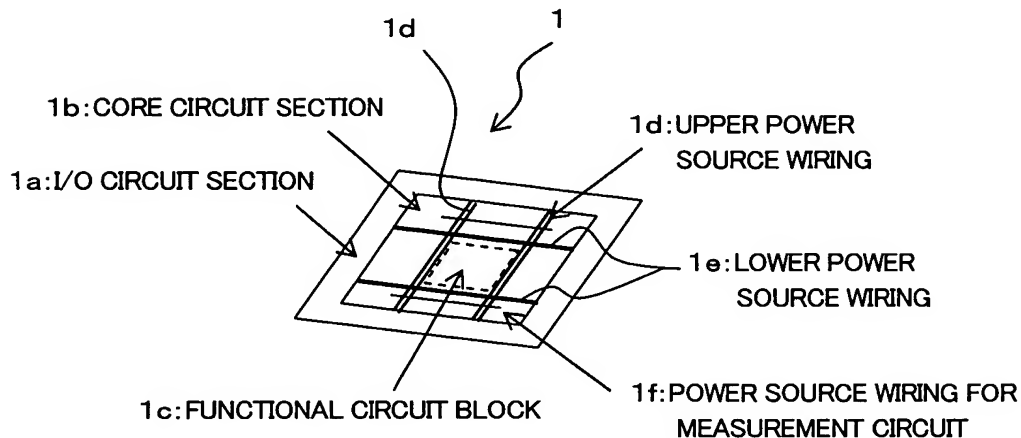


FIG. 13

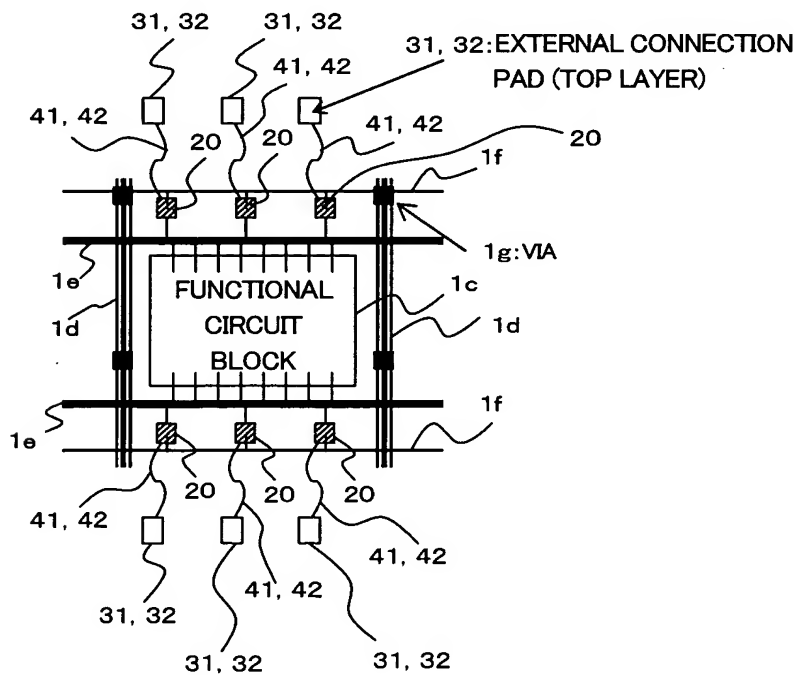


FIG. 14

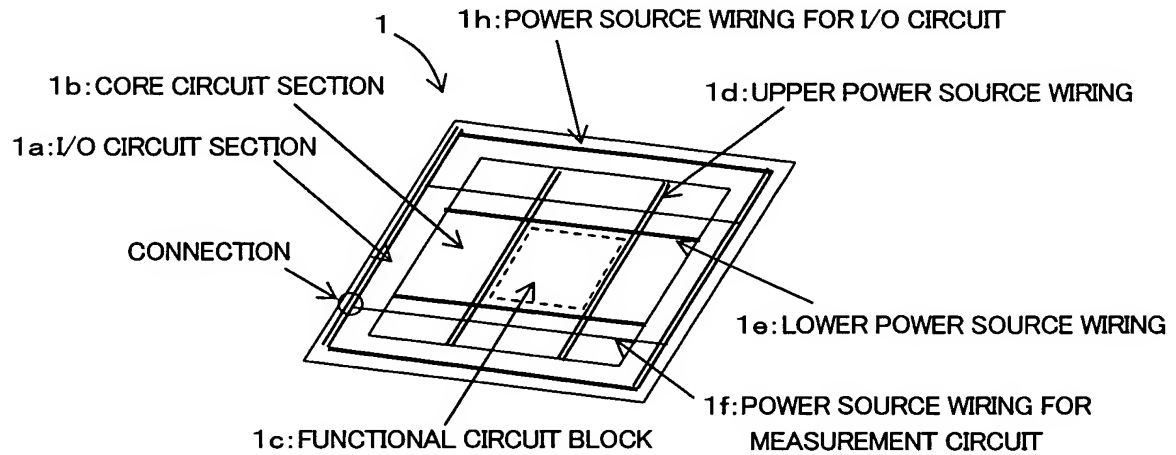


FIG. 15

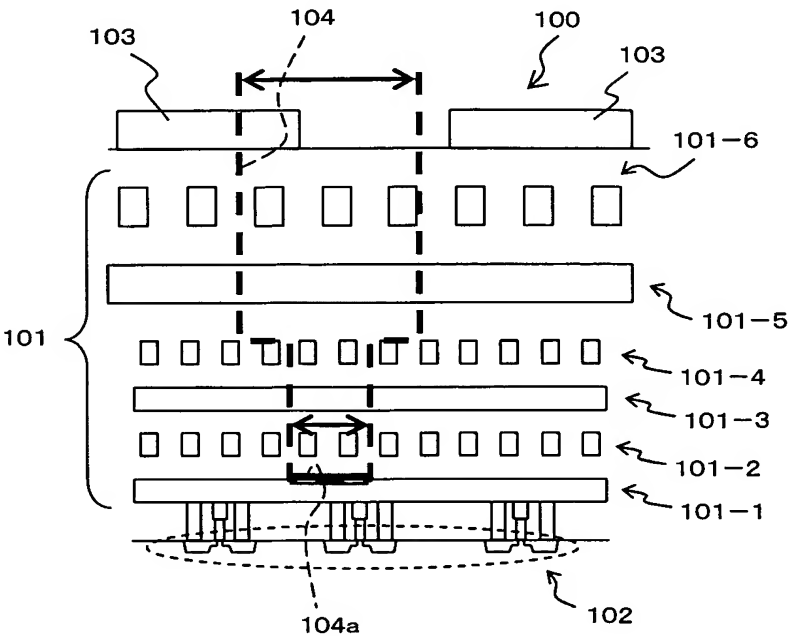


FIG. 16

